On-Chip EMC Issue: The Implementation of Patterned Ground Shields for Silicon Devices

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***Abstract*—This paper addresses some on-chip EMC issues for reducing power dissipation in the design of passive silicon-based devices operating at high frequencies. It is demonstrated that the implementation of patterned ground shields (PGS) together with differential technique can enhance the performance of spiral inductors, spiral transformers, and other devices effectively, which is compatible with standard CMOS fabrication technologies. However, the shielding effectiveness of a PGS is very sensitive to its embedding depth which should be chosen carefully. Some numerical results will be shown to demonstrate inductive couplings in various PGS inductors and transformers but are suppressed here.**

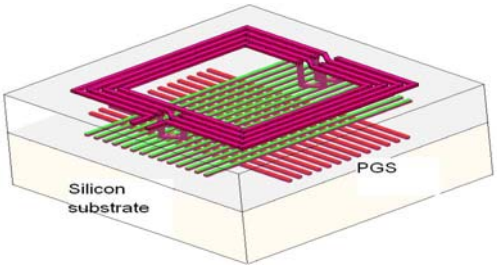
I. Introduction

As a traditional but very effective method, electric or magnetic shields have been widely used in various electrical and electronic systems so as to improve overall electromagnetic environments and reduce electromagnetic interferences. With the rapid development of advanced high-speed and radio frequency integrated circuits, both integration density and interconnection complexity are increased significantly. Under such circumstances, on-chip EMC becomes a very challenging issue, including power dissipation resulted from substrate loss, noise, coupling, crosstalk, and attenuation *etc*. In particular at high frequencies, all silicon-based passive as well as active devices suffer from serious substrate losses. For example, as operating frequency increases, the *Q*-factor of a spiral inductor or the maximum available gain of a spiral transformer will be reduced seriously. Further, it will result in degradation in performance of the circuit or system in which spiral inductors or transformers are employed.

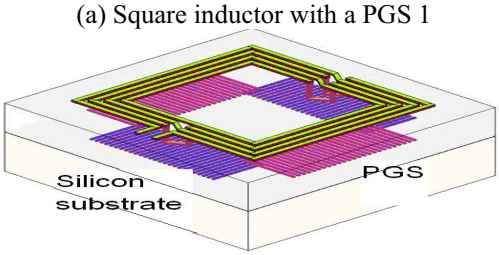
In this paper, the implementations of various patterned ground shields (PGS) together with differential technique in the design of silicon-based passive devices will be demonstrated experimentally. Due to the presence of PGS in silicon-based inductors or transformers, electromagnetic fields penetrated into silicon substrate are reduced, and therefore, their performances will be improved. However, the shielding effectiveness of a PGS is directly related to its embedding depth in silicon oxide layer.

II. On-Chip PGS Device Designs

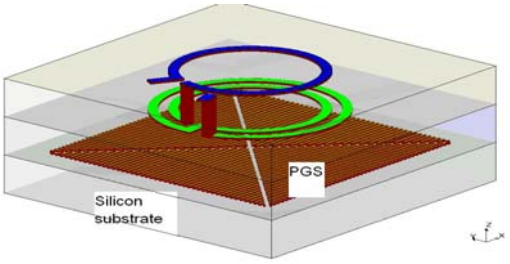
In the fabrication of silicon-based passive devices, such as coplanar waveguides, microstrip transmission lines, spiral inductors, and spiral transformers *etc*, a PGS can be easily implemented into the structure with not much fabrication cost increased. Figs. 1(a)-1(d) show some standard PGSs used before, which can be designed into different patterns [1]-[5].



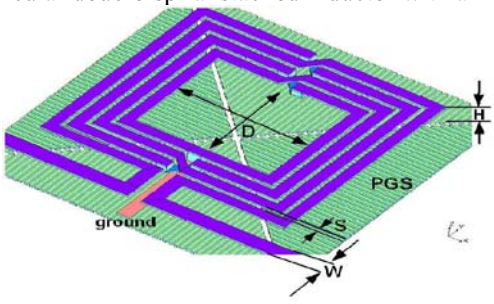
(a) Square inductor with a PGS 1



(b) Square inductor with a PGS 2

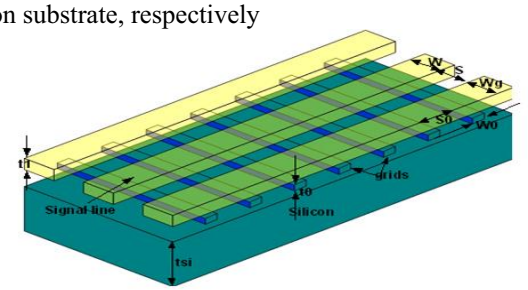


(c) Circular double-spiral stacked inductor with a PGS

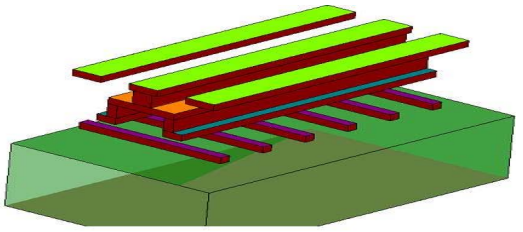


(d) Central-tapped transformer with a PGS

Fig.1. Three PGS inductors and a PGS transformer on a silicon substrate, respectively



(a)



(b)

Fig.2. Two coplanar waveguides with a patterned grid shield (PGS) on a silicon substrate, respectively.

In Figs. 1(a)-1(d), the introduced PGS will prevent electromagnetic energy to penetrate into silicon substrate. Therefore, eddy current loss in silicon substrate, in particular at high frequencies, will be reduced effectively. This means that the *Q*-factor of the PGS spiral inductor, the maximum available gain of the PGS transformer will be enhanced, respectively. However, it should be mentioned that the PGS will introduce additional parasitic capacitive coupling among metal spiral, PGS, and substrate, which will cause decrease of the self-resonance frequency of the inductor or transformer slightly. Hence, the embedding depth of a PGS should be chosen appropriately so as to suppress the effect of parasitic capacitance.

On the other hand, it should be mentioned that for silicon-based coplanar waveguides, we can take a similar way, as shown in Figs. 2(a) and 2(b）, by implementing a patterned grid shield (PGS) so as to reduce the substrate loss [6]-[9]. In Fig.2 (b), the signal line is designed into a novel form so as to increase its power handling capability and adjust its characteristic impedance.

All these passive PGS devices can be easily fabricated using standard CMOS technologies, and typically, their cross-sectional view is shown in Fig.3. An appropriate choice of the embedding depth of PGS, denoted by D, is very important in the effective implementation of a PGS, because it will introduce additional conductive power loss and capacitive coupling with silicon substrate and metal tracks.

For an on-chip PGS inductor, its performance can be described by its inductance L, Q-factor, and self-resonance frequency f_{res}, given by:

$$L = \frac{\mathrm{Im}[1/Y_{11}]}{\omega} \tag{1}$$

and

$$Q = \frac{\mathrm{Im}[Z_{in}]}{\mathrm{Re}[Z_{in}]} \tag{2}$$

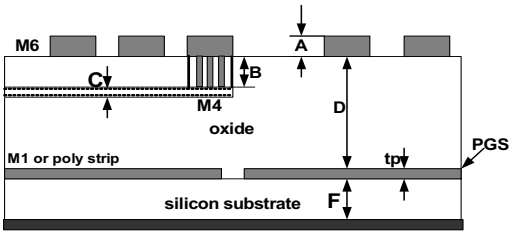


Fig.3. The implementation of a PGS in the design of an inductor or a transformer on a silicon substrate.

where Y_{11} and Z_{in} are one of the Y-parameters and input impedance which can be obtained from the measured two-port S-parameters. In the following section, it will be shown that the introduction of a PGS can increase the maximum *Q*-factor significantly，which is represented by $Q_{\max}$. The shielding effectiveness of a PGS can be defined by:

$$S_Q(dB) = 10\log\frac{Q_{\max}^{(PGS)}}{Q_{\max}^{(NPGS)}} \tag{3}$$

In the design of a PGS transformer, there are multiple choices in its configuration, such as interleaved, centre-tapped interleaved, and even stacked geometries. The performance parameters of a PGS transformer, such as maximum available gain ($G_{\max}$), self-resonance frequency, minimum noise figure ($NF_{\min}$), and power losses (P_{loss}) are directly related to its configuration. The $G_{\max}$ is defined by:

$$G_{\max}(T) = \left|\frac{S_{21}(T)}{S_{12}(T)}\right|\left(n - \sqrt{n^2-1}\right) \tag{4}$$

where

$$n = \frac{1 - |S_{11}(T)|^2 - |S_{22}(T)|^2 + |\Delta|^2}{2|S_{12}(T)S_{21}(T)|} \tag{5a}$$

and

$$\Delta = S_{11}(T)S_{22}(T) - S_{12}(T)S_{21}(T) \tag{5b}$$

or

$$G_{\max} = 1 + 2(x - \sqrt{x + x^2}) \tag{6a}$$

and

$$x = \frac{\mathrm{Re}(Z_{11}(T))\cdot\mathrm{Re}(Z_{22}(T)) - [\mathrm{Re}(Z_{12}(T))]^2}{[\mathrm{Re}(Z_{12}(T))]^2 + [\mathrm{Im}(Z_{12}(T))]^2} \tag{6b}$$

where T stands for the operating temperature, and we have taken the effects of possible rise in temperature into account on the performance of a PGS transformer.

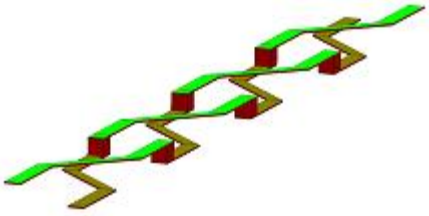
The minimum noise figure $NF_{\min}$ of a transformer is determined by

$$NF_{\min} = 10\log(1/G_{\max}) \quad (7)$$

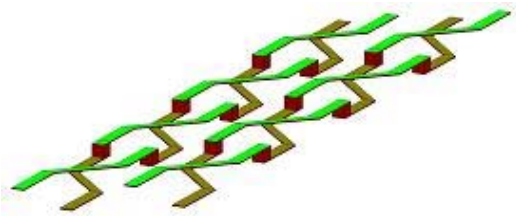
and the shielding effectiveness can be calculated by:

$$S_G(dB) = 10\log\frac{\max\{G_{\max}^{(PGS)}\}}{\max\{G_{\max}^{(NPGS)}\}} \quad (8)$$

On the other hand, it should be emphasized that differential techniques have been also used in the design of passive and active devices so as to suppress some electromagnetic interferences. More recently, some differential devices, such as differential coupled transmission lines (Figs.4(a) and 4(b)), differential inductors, and differential transformers have been proposed by some researchers [10].



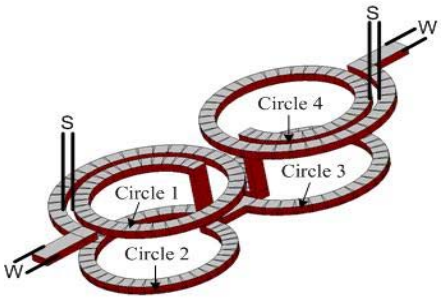
(a) Differential coupled transmission lines



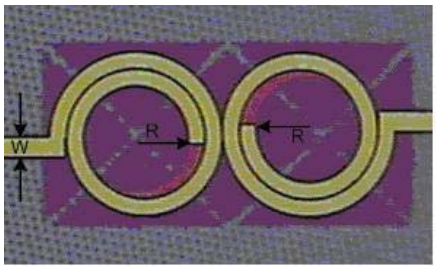
(b) A pair of differential coupled transmission lines

Fig.4. Differential coupled transmission lines

Here, the author would like to firstly demonstrate the geometry of one novel PGS differential spiral-stacked inductor fabricated using 0.18 μm CMOS technology, as shown in Fig. 5.



(a) Three-dimensional view without PGS



(b) Top view

Fig.5. Geometries of (a) no PGS and (b) PGS differential spiral-stacked inductor.

III. Simulation Methodologies

In order to fast and accurate capture frequency-dependent characteristics of the above on-chip PGS devices, circuit-oriented simulation method can be employed based on equivalent lumped-element circuit model, as shown in Fig. 6, for a square PGS transformer in Fig. 1(d)

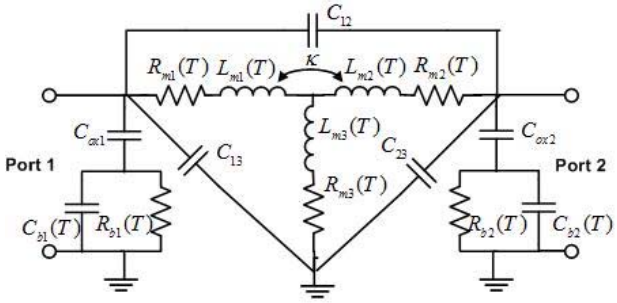
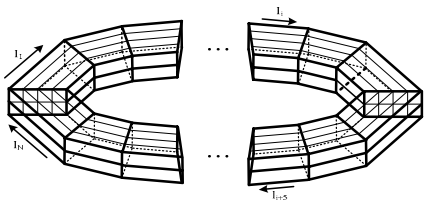
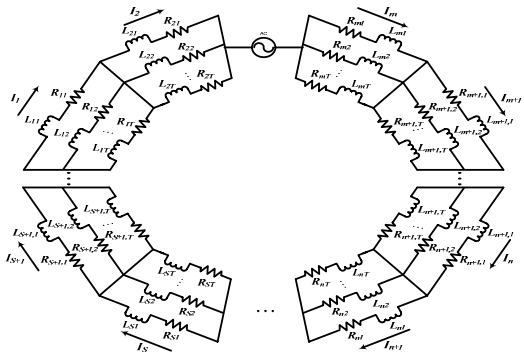


Fig.6. Equivalent lumped-element circuit model of a transformer

The values of most elements in Fig.6 can be obtained using some hybrid methods or extracted from the measured two-port S-parameters. For example, partial element equivalent circuit (PEEC) method can be used to calculate DC and AC resistances, or inductances of the spiral part, as shown in Figs. 7(a) and 7(b) briefly.



(a) Segmentation of a *N*-side regular polygon



(b) PEEC model

Fig.7. PEEC method used to calculate series resistance and inductance of a metal spiral.

In the PEEC method, the series resistance and inductance of the spiral part are calculated by a set of equations as follows:

$$R_s = \mathrm{Re}\left\{\sum_{i=1}^{S}\sum_{j=1}^{S} Z_{ij}\right\} \qquad L_s = \frac{1}{\omega}\mathrm{Im}\left\{\sum_{i=1}^{S}\sum_{j=1}^{S} Z_{ij}\right\} \quad \text{(9a, b)}$$

IV. Experimental Results and Discussion

As an example, Fig. 8 shows the *Q*-factor of a spiral-stacked inductor (Fig.5) as a function of frequency. In Fig.(8), empty square dotted line represents that both PGS and differential interconnect are implemented; and solid square dotted line corresponds to the case of non-PGS but with differential interconnect between two neighbouring stacked-spirals. It is evident that the combination of PGS and differential interconnect is a very effective way to improve the performance of a silicon-based on-chip inductor. For silicon-based transformers, similar conclusions can be drawn.

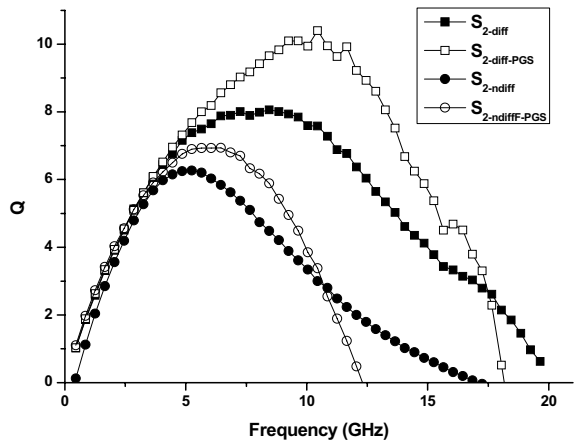


Fig. 8. The *Q*-factor of a spiral-stacked inductor as a function of frequency

V. Conclusions

In this paper, the author has addressed the method using patterned ground shields combined with differential interconnect to enhance the performance of silicon passive devices, which is completely compatible with CMOS fabrication technologies. Hence, this is an effective way to suppress on-chip electromagnetic interference and improve electromagnetic compatibility in the world of system-on-chip. Some numerical results will be demonstrated to show the effects of geometrical and physical parameters, *etc* on inductive and capacitive couplings in various PGS inductors and transformers.

Acknowledgment

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References

[1] C. P. Yue and S. S. Wong, "On-chip spiral inductors with patterned ground shields for Si-based RFIC's," *IEEE Journal of Solid-State Circuits,* vol. 33, no. 5, pp. 743-752, May 1998.

[2] S. M. Yim, T. Chen, and K. O. Kenneth, "The effects of a ground shield on the characteristics and performance of spiral inductors," *IEEE Journal of Solid-State Circuits,* vol. 37, no. 2, pp. 237-244, Feb. 2002.

[3] C. A. Chang, S. P. Tseng, J. Y. Chung, S. S. Jiang, and J. A. Yeh, "Characterization of spiral inductors with patterned floating structures," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-52, no. 5, pp. 1375-1381, May 2004.

[4] Tak Shun Dickson Cheung, and J. R. Long, "Shielded passive device for silicon-based monolithic microwave and millimeter-wave integrated circuits," *IEEE J. Solid-State Circutis,* vol. 41, no.5, pp. 1183 – 1200, May 2006.

[5] J. L. Shi, W. Y. Yin, K. Kang, J. F. Mao, and L. W. Li, "Frequency-thermal characterization of on-chip transformers with patterned ground shields," *IEEE Trans. Microwave Theory Tech.*, vol. 55, no. 1, pp. 1–12, Jan. 2007.

[6] C. Chien, A, F. Burnett, J. M. Cech, and M. H. Tanielian, "The signal transmission characteristics of embedded microstrip transmission lines over a meshed ground plane in copper/polyimide multichip module," *IEEE Trans. Comp., Hybrids, Maufact. Technol*., vol. 17, pp. 578-583, 1994.

[7] R. Lowther and S. G. Lee, "On-chip interconnect lines with patterned ground shields," *IEEE Microwave Wireless Components Lett.*, vol. 10, no. 2, pp. 49-51, 2000.

[8] R. D. Luth, V. K. Tripathi, and A. Weisshaar, "Enhanced transmission characteristics of on-chip interconnects with orthogonal gridded shield," *IEEE Trans. Advanced Packaging*, vol. 34, pp. 288-293, 2001.

[9] P. Wang and E. C. C. Kan, "High-speed interconnects with underlayer orthogonal metal grids," *IEEE Trans. Advanced Packaging*, vol. 27, no. 3, pp. 497-507, 2004.

[10] J. Chen, and J. J. Liu, "Modeling of on-chip differential inductors and transformers/baluns," *IEEE Trans. Electron Devices*, vol. 54, no. 2, pp. 369–371, Feb. 2007.